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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,432	07/31/2003	Jeffrey P. Rupley II	42P16353	2860

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EXAMINER	
MOLL, JESSE R	
ART UNIT	**PAPER NUMBER**
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/632,432	RUPLEY ET AL.	
	Examiner	Art Unit	
	Jesse R. Moll	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-22* is/are allowed.

6)☒ Claim(s) *23-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 23-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Eickemeyer et al. (U.S. Patent No. 6393552 B1) herein referred to as Eickemeyer.

3. Regarding claim 23, Eickemeyer discloses an apparatus comprising: a storage structure to store at least one entry (fig. 3, ref. 313), the at least one entry to include a register type identifier value (fig, 3, ref. 335; col. 4, lines 53-57; the sector mask indicates the type of register stored in that location [32 or 64 bit]); a first physical rename register of a first type (fig. 3, ref. RR1A; col. 3, lines 55-60), the first type having a first length (32-bit); and a second physical rename register of a second type(fig. 3, ref. RR1; col. 3, lines 55-61), the second type having a second length different than the first length (64-bit;

> *Note that if both status bits are set, the processor renames using the RR1 register (which is 64 bits long); otherwise, it uses the RR1A register (which is 32 bits long). Further note that the registers RR1 and RR1A do share common bits, however, the application does not explicitly claim that the registers cannot share bits.*);

and rename logic to map an instance of the logical register to a selected one of the physical rename register (

Note that the logical register AR1 can be mapped to any of the rename registers RRN if the entire 64 bits need to be mapped or any of the registers RRNA if only 32 bits need to be mapped.)

dependant upon the number of bits (32 or 64) of the logical predicate register (any register can be used as a predicate) that are to be written by a current instruction (whichever instruction writes to that register;

Note that the rename logic will either map the register to a single sector of the register (first register) or to both sectors (second register) dependent on the size of the register being written.),

the rename logic further to place a register type identifier into the storage entry to indicate the type of the selected physical rename register (see fig. 3, ref. 335, col. 4, lines 53-57 regarding the sector mask; also see above regarding the register type identifier value).

4. Regarding claim 24, Eickemeyer discloses the apparatus of claim 23, wherein: the first and second physical rename registers belong to a plurality of t physical renamge registers, wherein t > 2. (col. 3, lines 54-61).

Note that the plurality of registers includes all 32-bit registers in the first sector (RR1A-RRnA & RR1B-RRnB) and all of the full 64-bit registers.

5. Regarding claim 25, Eickemeyer discloses the apparatus of claim 23, wherein: the storage structure is to store a plurality of entries (registers), each of the plurality of entries to include a corresponding register type identifier value (Sector Mask, see above regarding claim 1)

Note each entry in the rename file has (when in use) a corresponding entry in the rename table. The entry in the rename table contains the register type identifier value.

6. Regarding claim 26, Eickemeyer discloses the apparatus of claim 23, wherein: the first physical rename register is one of a plurality (z) of physical rename registers of the first length (RR1A, RR1B, RR2A, RR2B, RR3A...)

7. Regarding claim 27, Eickemeyer discloses the apparatus of claim 23, wherein: the second physical rename register is one of a plurality (m) of physical rename registers of the second length (RR1, RR2, RR3...)

8. Regarding claim 28, Eickemeyer discloses the apparatus of claim 26, wherein: the second physical rename register is one of a plurality (m) of physical rename registers of the second length (RR1, RR2, RR3...)

9. Regarding claim 29, Eickemeyer discloses the apparatus of claim 28, wherein: z is not equal to m (there are twice as many 32-bit registers as 64-bit registers).

10. Regarding claim 30, Eickemeyer discloses the apparatus of claim 24, wherein the selected physical rename register is selected from the plurality of n registers, which includes multiple registers of both the first type and the second type (col. 3, lines 54-61).

Note that the logical register AR1 can be mapped to any of the rename registers RRN if the entire 64 bits need to be mapped or any of the registers RRNA if only 32 bits need to be mapped.

Allowable Subject Matter

11. Clams 9-22 are allowed. Please refer to the Office Action mailed 17 August 2006 which sets forth the reasons for allowance.

Response to Arguments

12. Applicant's arguments filed 8 March 2007 have been fully considered but they are not persuasive. Applicant states:

> When rejecting independent claim 23, the Examiner asserted that the "sector mask" disclosed in Eickemeyer (fig. 3, ref. 335; col. 4, lines 53-57) is the same or equivalent to the "register type identifier value" recited in claim 23. Col. 4, lines 53-57 of Eickemeyer is quoted below:
>
> The first column 331 in the Rename Table 313 contains the architected register number, the second column 333 contains the instruction address and the third column 335 contains architected register or rename register number plus the sector mask. There is one sector mask bit for each sector.
>
> Applicants cannot find where in the above quoted portion of Eickemeyer discloses that the sector mask indicates the type of register stored on that location, as asserted by the Examiner in the Office Action. In fact, Applicants read the entire Eickemeyer reference and it does not expressly disclose what a sector mask is and what information it represents. When making the above assertion, the Examiner must have relied on some knowledge outside Eickemeyer. Applicants respectfully request that the Examiner point out whatever knowledge the Examiner relied on in making this assertion so that a determination may be made regarding whether that knowledge source is common to a person having ordinary skill in the art. Without such a supplemental knowledge source outside Eickemeyer, Applicants must assume that the sector mask disclosed in Eickemeyer is not the same or equivalent to the register type Identifier value recited In claim 23 and hence that the "register type identifier value" element in claim 23 is not taught by Eickemeyer.

Examiner disagrees. The term "register type identifier value" is reasonably and broadly interpreted as a value which identifies a register type. The two sector mask bits indicate which sectors are being used. If two sectors are being used (mask bits = 11), it a 64-bit register and a 32-bit register if one sector is being used (mask bits = 01 or 10). These two situations are clearly different types of registers (32-bit and 64-bit) so the

sector mask is clearly a value which identifies a register type and therefore a "register type identifier value".

13. Applicant's arguments filed 8 March 2007 have been fully considered but they are not persuasive. Applicant states:

> Additionally, the Examiner asserted that AR1 as disclosed in Eickemeyer (see fig. 1; col. 3, lines 45-47) is a logical register. Applicants respectfully disagree. Eickemeyer expressly discloses that Architected Register File (ARF) 301 is a component of CPU (see col. 3, lines 43-47 of Eickemeyer) which Indicates that ARF is a physical register file. That ARF is a physical register file can further be supported by col. 4, lines 14-20 or Eickemeyer as quoted below:
>
> The renaming register pool, i.e. the group of registers available for renaming, consists of a number .of 32-bit registers. These rename registers arc used independently for each 32-bit register sector that needs to be renamed. This po01 consists of A sectors 309 and B sectors 311 in the RRF 300, and A sectors 305 in the ARF 307.
>
> The above quoted portion of Eickemeyer dearly shows that ARF is treated in the same way as the Rename Register File (RRF): both of them can be renamed. There is no doubt that RRF is a physical register. Thus, ARF is also a physical, register, if the Examiner insists that ARFI particularly AR1, is a logical register, Applicants respectfully request that the Examiner provide clear evidence showing so.

Examiner disagrees. As Eickemeyer states (col. 4, lines 1-13), register renaming is used. Since registers (logical registers) are mapped to the RRF (physical registers), a logical register must exist. Because renaming occurs, logical registers must exist (which are mapped to the physical registers in the RRF and the ARF). Specific instances (at distinct positions of processing a program) of the architectural registers (including AR1) are mapped to the register files inherently in any system using register renaming.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

15. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571)272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
Art Unit 2181

JM 7/22/2007

ALFORD KINDRED
PRIMARY EXAMINER